

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0004] on page 1, beginning on line 9 with the following amended paragraph:

In [0004]A typical phase locked loop (PLL) system, including a phase detector, a charge pump, a loop filter, a voltage-controlled oscillator (VCO) and divider, generally uses [[a]],the voltage-controlled oscillator (VCO) to produce required frequencies. As shown in FIG. 1A, the VCO 10 includes a series of n-stage voltage control delay lines (VCDL), each stage having a control terminal, an output terminal, and an input terminal. Take the i-th stage VCDL as an example, the i-th stage VCDL has a control terminal coupled to a common voltage control signal Vc for outputting an oscillating signal to an input terminal of the (i+1)th stage VCDL in a delay time  $T_i(V_c)$ . An output terminal of the n-th stage VCDL is coupled to an input terminal of the first stage VCDL and outputs an oscillating signal with a central frequency  $\frac{1}{2 \times \sum_{k=1}^n T_k(V_c)}$ . It is noted that each stage VCDL has a specific delay time represented by a function of voltage control signal Vc.